Woori-Net	Issue Date(Final revised) 2022.03.22	Document Number 1	Document Version 1.5
Issued by(Last revised)	Reviewed by	Approved by	Document Administrator

WM-N500JSE

Hardware Manual

Version 1.5

Contents

■ Revision History

All revisions made to this document are listed below;

Version	Date	Description	Issued by
1.4	2021-12-20	*Initial release for Soft Bank in Japan*	Alex choi
1.5	2022-03-22	Update User guide	MY Cho

1. Product Overview

1.1. WM-N500JSE series:

- ✓ Qualcomm MDM9206 chipset

<Model name and Features>

Model Name	Carrier	LTE BAND	CATEGORY	MEMORY (MCP)	S/W
WM-N502JS		B1, B8	M1 only	4Gb NAND Flash / 2Gb DDR2	Linux

Frequency bands:

- ✓ LTE B1 – TX : 1920 ~1980MHz, LTE – RX : 2110~2170MHz MHz
- ✓ LTE B8 – TX : 880~915MHz, LTE – RX : 925~960MHz

1.2. Contents and Function

1) Model Name: WM-N500JSE
2) Target User: IoT Users
3) Network:
   - ✓ Data only
   - ✓ LTE Cat.M1 : Band8, Band1
   - ✓ GPS(Optional): 1574.4MHz ~ 1605.9MHz
4) RF Power: Power Class III

2. Product Specification and Characteristics

2.1. HW / Dimension

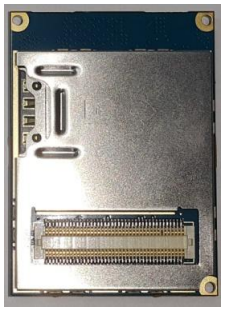
<HW Features>

Items	Specifications	Remark
Chipset	Qualcomm MDM9206	
Memory (MCP)	NAND Flash+ DDR2	
USIM Interface	External USIM (PIN OUT)	
Connectivity	UART 2EA / SPI 1EA / I2C 1 EA GPIO USB 2.0 / UIM / JTAG	
Air Interface	LTE : Band1 , Band8	
Antenna	PIN OUT Type	
Power consumption (Max. current)	550 mA (@ Tx Max Power 23dBm ±0.4dB, +4.0V)	@ LTE B8
Operating Voltage	+3.4 Vdc ~ +4.2 Vdc	
Dimension / Weight	26.6 x 28.0 X 2.7 (mm) (aprox. 6.8g)	
Operating Temperature & Humidity	-20℃ ~ +60℃ / 95% (@+60℃)	

2.2. Exterior photos

.

< TOP >



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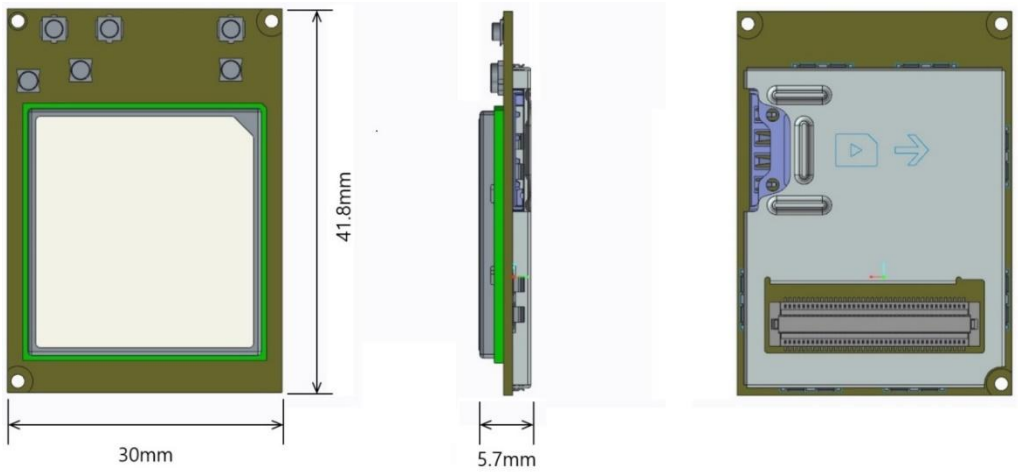
<Picture 2.2 WM-N500JSE Exterior photos >

2.3. Exterior Drawing



<Picture 2.3 WM-N500JSE 외관 도면>

2.4. Module characteristic

2.4.1. electrical characteristic

<Chart 2.4.1 electrical characteristic>

Parameter	Description	Min.	Typ.	Max.	Units
V_Batt	Power Supply Voltage	3.4	4.0	4.2	V
Iv_batt	Power Supply Current	550	-		mA
Traffic current	Power save mode (PSM)	-	7.3	-	uA
	IDLE	-	0.79	-	mA
	Tx Max Power 23dBm ±0.4dB, +4.0V)	450	500	550	mA
Power off	Average of power off current consumption	5.3		10	uA
VIH	High-level Input Voltage, CMOS	1.17	1.8	2.1	V
VIL	Low-level Input Voltage, CMOS	-0.3	-	0.63	V
VOH	High-level Output Voltage, CMOS	1.35	-	1.8	V
VOL	Low-level Output Voltage, CMOS	0	-	0.45	V

2.4.2. Reliability characteristic

<Chart 2.4.2 Reliability characteristic>

ITEM	Specification
Storage Temperature	-40℃ to + 85℃
Operating Temperature	-20℃ to + 60℃
Humidity (Operating)	95%(60℃) relative humidity (non-condensing)
Vibration (Operating)	10 Hz to 100 Hz sinusoidal, 1.0G
Drop	No damages after 75cm drop over concrete floor

2.4.3. RF characteristic

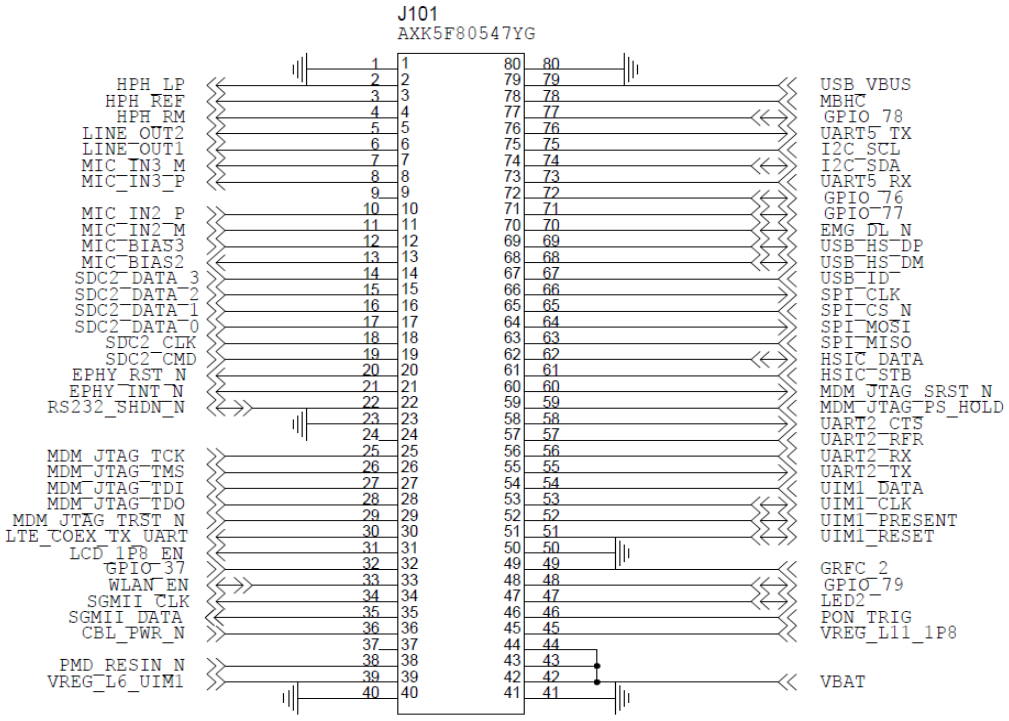
<Chart 2.4.3 RF characteristic>

ITEM	Condition				Specification
	BW	DL conf	UL conf		
			Mod	RB	
Maximum Output Power (Class 3)	1.4MHz 3MHz 5MHz 10MHz 15MHz 20MHz	NA	QPSK	5MHz 1 RB 10MHz 1,4 RB 15MHz 1,6 RB 20MHz 1,6 RB	+23 dBm ±2.7dB

Minimum Output Power	1.4MHz 3MHz 5MHz 10MHz 15MHz 20MHz	NA	QPSK	5MHz 6 RB	< -40 dBm
Frequency Error	5MHz	QPSK 4RB	QPSK	6 RB	±0.1ppm @ Band 5,8 ±0.2ppm @ Band 1,3
EVM	5MHz	NA	QPSK	1,6 RB	< 17.5%
			16QAM	1,5 RB	< 12.5%
Maximum Input Level	5MHz	16QAM 2RB	QPSK	6	> -25.7dBm
Reference Sens. Level	5MHz	QPSK 4RB	QPSK	6	< -102.3dBm @ Band1 < -99.3dBm @ Band3 < -100.8dBm @ Band5 < -99.8dBm @ Band8

✓ RF Spec 3GPP TS36.521 Support.

2.5. Pin Assignment



<Picture 2.5 WM-N500JSE Pin Assignment>

2.6. I/O parameter definitions

<Chart 2.6 WM-N500JSE I/O parameter definitions >

Symbol	Description
Pad attribute	
PI	Power input
PO	Power output

B	Bidirectional digital
DI	Digital input
DO	Digital output
AI	Analog input
AO	Analog output
AIO	Analog input, output
Pad voltage	
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (2.85 V),
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.8 V or 2.85 V)
P6	Pad group 6 (UIM2 and MDIO); tied to VDD_P6 pins (1.8 V or 2.85 V)
P8	Pad group 8 (HSIC); tied to VDD_P8 pins (1.2 V)

2.7. Pin Description

<Chart 2.7 WM-N500JSE Pin Description >

Signal Name	PAD No.	I/O	Voltage	Functional description
Power				
VBAT	42,43,44	PI	4.0V	Main Power Supply
GND	1,23,40,41,50,80	-	-	Ground

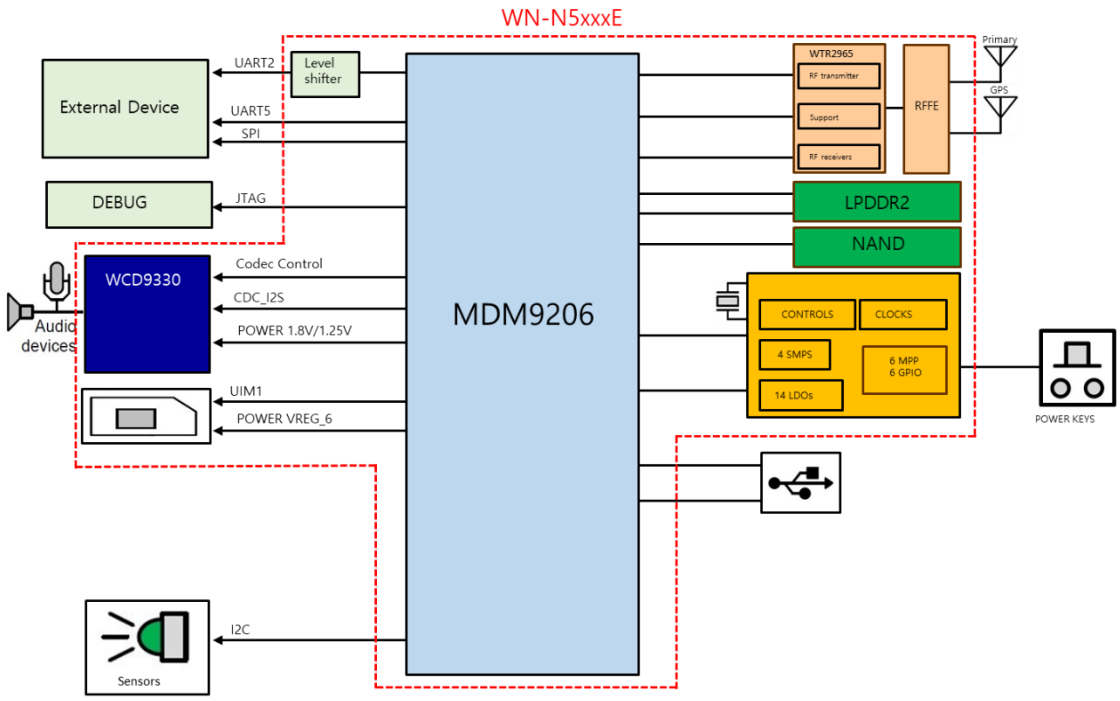
VREG_L11_1P8	45	PO	P3	1.8V Regulated Voltage for reference voltage or customer's use case
Power Control				
CBL_PWR_N	36	DI	-	Power On Signal (Active Low)
PMD_RESIN_N	38	DI	-	Reset/
UART Interface				
UART2_TX	55	DO	2.85V	UART TX
UART2_RX	56	DI	2.85V	UART RX
UART2_CTS	58	DI	2.85V	UART CTS
UART2_RFR	57	DO	2.85V	UART RFR
UART5_TX	76	DO	P3	UART TX
UART5_RX	73	DI	P3	UART RX
SPI Interface				
SPI_MOSI	64	DO	P3	SPI_MOSI
SPI_MISO	63	DI	P3	SPI_MISO
SPI_CS_N	65	DO	P3	SPI_CS_N
SPI_CLK	66	DO	P3	SPI_CLK
External USIM Interface				
VREG_L6_UIM1	39	PO	P5	External USIM Power
UIM1_RESET	51	DO	P5	External USIM Reset
UIM1_PRESENT	52	DI	P3	External USIM Detect
UIM1_CLK	53	DO	P5	External USIM Clock
UIM1_DATA	54	B	P5	External USIM Data
USB Interface				
USB_VBUS	79	PI	5V	USB Power Supply
USB_ID	67	AI	-	USB High speed ID
USB_HS_DM	68	AIO	-	USB High-speed differential data (-)

USB_HS_DP	69	AIO	-	USB High-speed differential data (+)
SDIO Interface				
SDC2_DATA3	14	B	P2	Secure digital controller2 databit3
SDC2_DATA2	15	B	P2	Secure digital controller2 databit2
SDC2_DATA1	16	B	P2	Secure digital controller2 databit1
SDC2_DATA0	17	B	P2	Secure digital controller2 databit0
SDC2_CLK	18	B	P2	Secure digital controller2 clock
SDC2_CMD	19	B	P2	Secure digital controller2 command
I2C Interface				
I2C_SDA	74	B	P3	I2C data
I2C_SCL	75	B	P3	I2C Clock
JTAG Interface				
MDM_JTAG_PS_H	59	DI	P3	JTAG PSHOLD
MDM_JTAG_SRST_	60	DI	P3	JTAG reset for debug
MDM_JTAG_TCK	25	DI	P3	JTAG clock input
MDM_JTAG_TMS	26	B	P3	JTAG mode select input
MDM_JTAG_TDI	27	DI	P3	JTAG data input
MDM_JTAG_TDO	28	DO	P3	JTAG data output
MDM_JTAG_TRST_	29	DI	P3	JTAG reset
GPIO				
LED2	47	DO	1.8V	GPIO for Power monitor LED control
GPIO_37	32	DO	P3	GPIO for LED control
RS232_SHDN_N	22	DO	1.8V	GPIO for RS232 shutdown
EMG_DL_N	70	DI	P3	Emergency Download key input wakeup interrupt GPIO
GPIO_76	72	DO	P3	General GPIO
GPIO_77	71	DO	P3	General GPIO

GPIO_78	77	DO	P3	General GPIO
GPIO_79	48	DO	P3	General GPIO
ETC				
NC	9,24,37,	-	-	No internal connection
HPH_LP	2	-	-	These pins are reserved for specific application. It needs to be discussed for use cases.
HPH_REF	3	-	-	
HPH_RM	4	-	-	
LINT_OUT2	5	-	-	
LINE_OUT1	6	-	-	
MIC_IN3_M	7	-	-	
MIC_IN3_P	8	-	-	
MIC_IN2_P	10	-	-	
MIC_IN2_M	11	-	-	
MIC_BIAS3	12	-	-	
MIC_BIAS2	13	-	-	
EPHY_RST_N	20			
EPHY_INT_N	21	-	-	
LTE_COEX_TX_UAR	30	-	-	
LCD_1P8_EN	31	-	-	
WLAN_EN	33	-	-	
SGMII_CLK	34	-	-	
SGMII_DATA	35	-	-	
PON_TRIG	46	-	-	
GRFC_2	49	-	-	
HSIC_STB	61	-	-	
HSIC_DATA	62	-	-	
MBHC	78	-	-	

3. Block Diagram

3.1. Application & System Block diagram



<Picture 3.1 WM-N500JSE Block diagram >

4. System Interface

4.1. Modem Power supply

<Chart 4.1 WM-N500JSE Power interface >

PAD No.	Signal Name	I/O	Voltage(Typ.)	Functional description
42	VBAT	PI	4.0V	External Power Supply
43	VBAT	PI	4.0V	External Power Supply
44	VBAT	PI	4.0V	External Power Supply
45	VREG_L11_1P8	AO	P3	1.8V Regulated Voltage for reference voltage or customer's use case

4.2. Modem Power Control (Power on/off)

<Chart 4.2 WM-N500JSE Power control interface >

PAD No.	Signal Name	I/O	Voltage(Typ.)	Functional description
36	CBL_PWR_N	DI	0.8~1.0V	Power On Signal (Active Low)

38	PMD_RESIN_N	DI		HW Reset (Active Low)

4.3. UART Interface

UART2 : Support AT command .

UART5 : Support Console UART.

<Chart 4.3 WM-N500JSE UART interface >

PAD No.	Signal Name	I/O	Voltage	Functional description
UART2 : Modem AT command UART				
55	UART2_TX	DO	2.85V	High-speed UART transmit data output
56	UART2_RX	DI	2.85V	High-speed UART receive data input
58	UART2_CTS	DI	2.85V	High-speed UART clear to send signal
57	UART2_RFR	DO	2.85V	UART1 ready for receive signal
UART5 : Console UART				
76	UART5_TX	DO	P3	Uart Tx
73	UART5_RX	DI	P3	Uart Rx

4.4. SPI Interface

<Chart 4.4 WM-N500JSE SPI interface >

PAD	Signal Name	I/O	Voltage	Functional description

64	SPI_MOSI	DO	P3	SPI_MOSI
63	SPI_MISO	DI	P3	SPI_MISO
65	SPI_CS_N	DO	P3	SPI_CS_N
66	SPI_CLK	DO	P3	SPI_CLK

4.5. External USIM Interface

<Chart 4.5 WM-N500JSE USIM interface >

PAD No.	Signal Name	I/O	Voltage	Functional description
39	VREG_L6_UIM1	PO	P5	USIM Power
51	UIM1_RESET	DO	P5	USIM Reset
52	UIM1_PRESENT	DI	P3	UIM Detection
53	UIM1_CLK	DO	P5	UIM Clock
54	UIM1_DATA	B	P5	UIM Data

4.6. USB Interface

WM-N500JSE modem supports USB2.0 HS.

<Chart 4.6 WM-N500JSE USIM interface >

PAD	Signal Name	I/O	Voltage	Functional description
79	USB_VBUS	PI	5V	USB Power Supply
67	USB_ID	AI	-	USB ID
68	USB_HS_DM	AIO	-	High-speed USB differential data, (-) side
69	USB_HS_DP	AIO	-	High-speed USB differential data, (+) side

4.7. SDIO Interface

<Chart 4.7 WM-N500JSE SDIO interface >

PAD	Signal Name	I/O	Voltage	Functional description
14	SDC2_DATA3	B	P2	Secure digital controller2 databit3
15	SDC2_DATA2	B	P2	Secure digital controller2 databit2
16	SDC2_DATA1	B	P2	Secure digital controller2 databit1
17	SDC2_DATA0	B	P2	Secure digital controller2 databit0
18	SDC2_CLK	B	P2	Secure digital controller2 clock
19	SDC2_CMD	B	P2	Secure digital controller1 command

4.8. I2C Interface

<Chart 4.8 WM-N500JSE I2C interface >

PAD	Signal Name	I/O	Voltage	Functional description
74	I2C_SDA	B	P3	I2C data
75	I2C_SCL	B	P3	I2C Clock

4.9. JTAG Interface

<Chart 4.9 WM-N500JSE JTAG interface >

PAD	Signal Name	I/O	Voltage	Functional description
59	MDM_JTAG_PS_HOLD	DI	P3	JTAG PSHOLD
60	MDM_JTAG_SRST_N	DI	P3	JTAG reset for debug
25	MDM_JTAG_TCK	DI	P3	JTAG clock input

26	MDM_JTAG_TMS	B	P3	JTAG mode select input
27	MDM_JTAG_TDI	DI	P3	JTAG data input
28	MDM_JTAG_TDO	DO	P3	JTAG data output
29	MDM_JTAG_TRST_N	DI	P3	JTAG reset

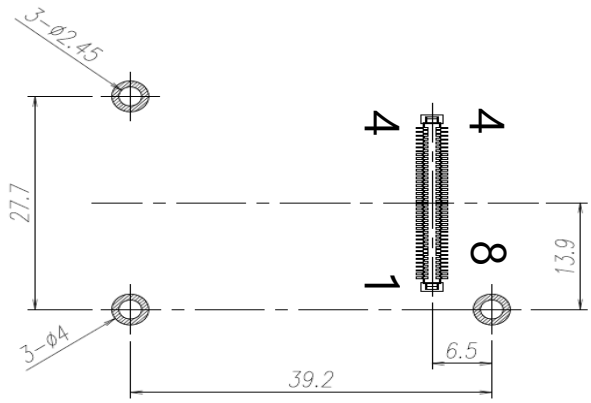
4.10 GPIO Interface

<Chart 4.10 WM-N500JSE GPIO interface >

PAD	Signal Name	I/O	Voltage	Functional description
47	LED2	DO	1.8V	GPIO for Power monitor LED control
32	GPIO_37	DO	P3	GPIO for LED control
22	RS232_SHDN_N	DO	1.8V	GPIO for RS232 shutdown
70	EMG_DL_N	DI	P3	Emergency Download key input
72	GPIO_76	DO	P3	General GPIO
71	GPIO_77	DO	P3	General GPIO
77	GPIO_78	DO	P3	General GPIO
48	GPIO_79	DO	P3	General GPIO

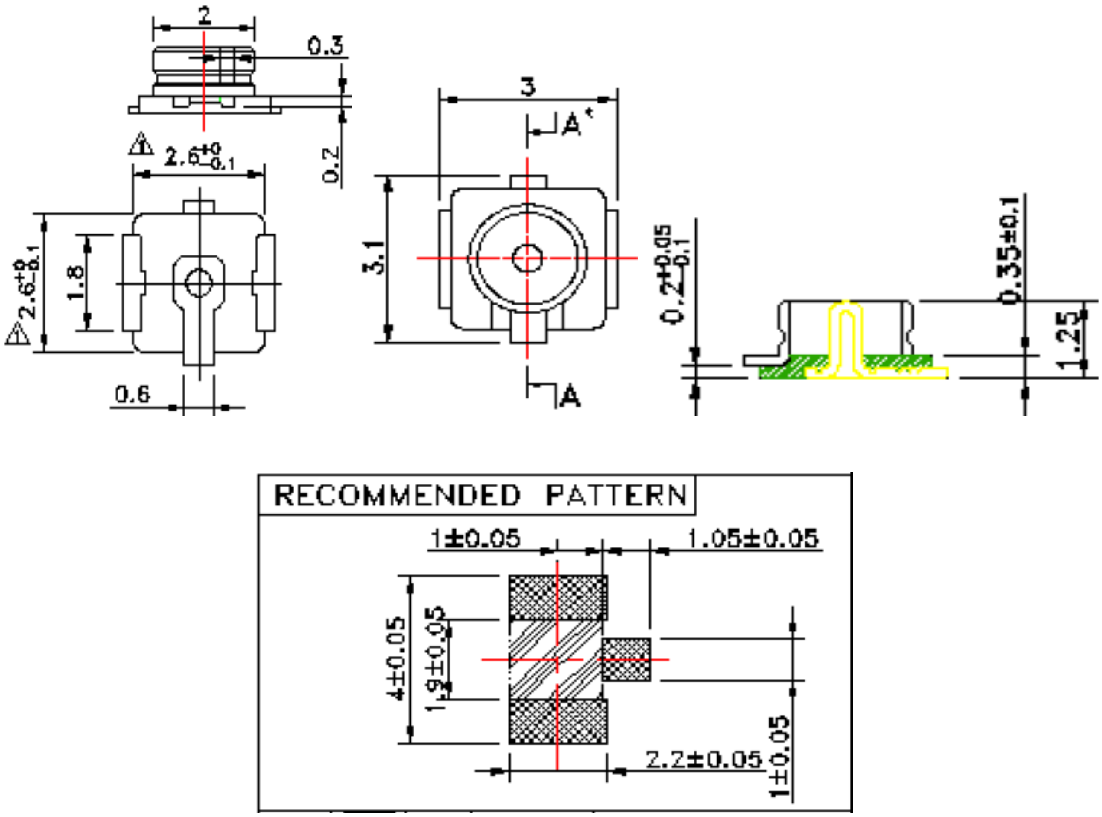
5. PCB Layout Guide

5.1. PCB Layout



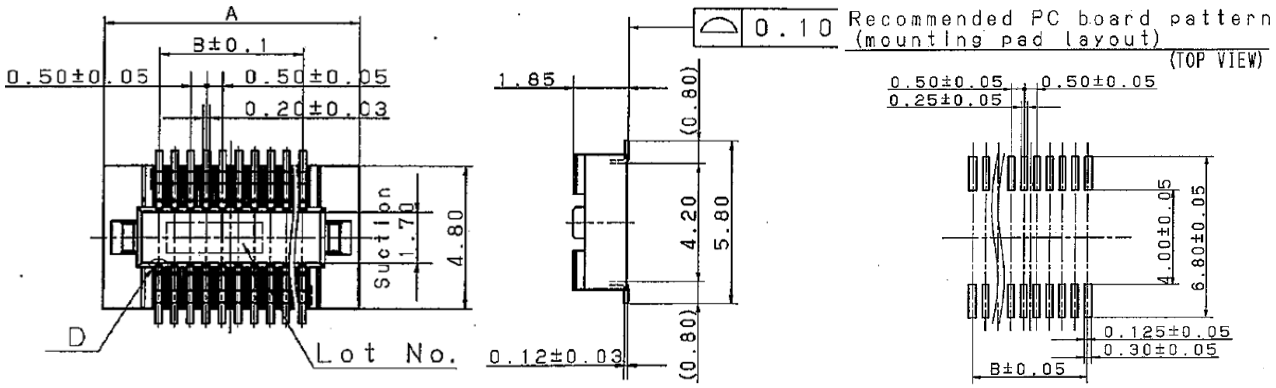
<Picture5.1 WM-N500JSE PCB LAND PATTERN >

5.2. CMJ Connector Specification

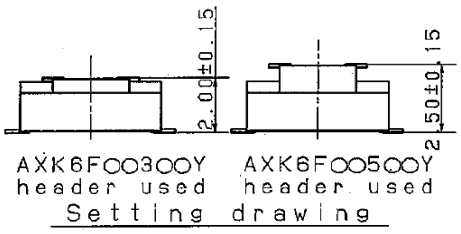


<Picture5.2 Gigalane 社, CMJ-S01-501 >

5.3. 80 Pin Connector Specification

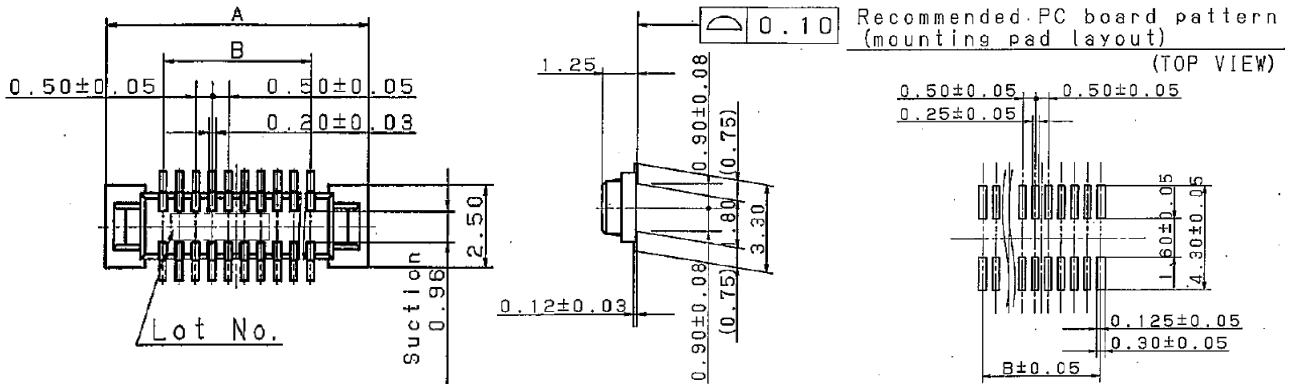


Dimension / No. of contacts	A	B
10	5.50	2.00
12	6.00	2.50
14	6.50	3.00
16	7.00	3.50
18	7.50	4.00
20	8.00	4.50
22	8.50	5.00
24	9.00	5.50
26	9.50	6.00
30	10.50	7.00
34	11.50	8.00
40	13.00	9.50
50	15.50	12.00
60	18.00	14.50
70	20.50	17.00
80	23.00	19.50
100	28.00	24.50

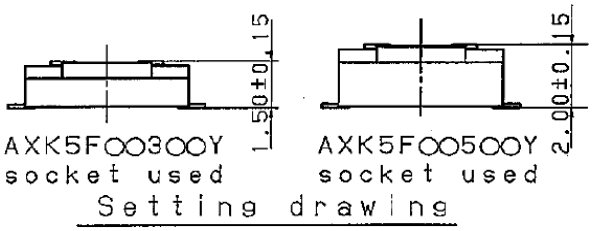


<Picture5.3 PANASONIC 社, AXK5F80547YG : Socket>

5.4. 80 Pin Connector Specification

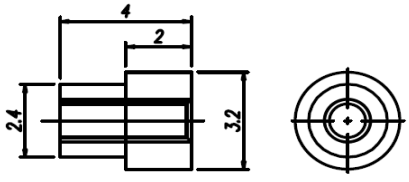


Dimension / No. of contacts	A	B
10	5.50	2.00
12	6.00	2.50
14	6.50	3.00
16	7.00	3.50
18	7.50	4.00
20	8.00	4.50
22	8.50	5.00
24	9.00	5.50
26	9.50	6.00
30	10.50	7.00
32	11.00	7.50
34	11.50	8.00
40	13.00	9.50
50	15.50	12.00
60	18.00	14.50
70	20.50	17.00
80	23.00	19.50
100	28.00	24.50



<Picture5.4 PANASONIC 社, AXK6F80347YG : Header>

5.5. Insert nut & screw



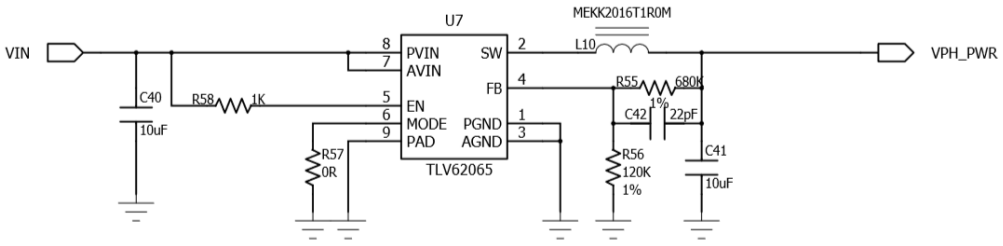
screw spec.: M1.4X3.0 D2.5 T0.5 Machine

<Picture5.5 Insert nut & screw >

-EOD-

6. User Guide

6.1 Power supply

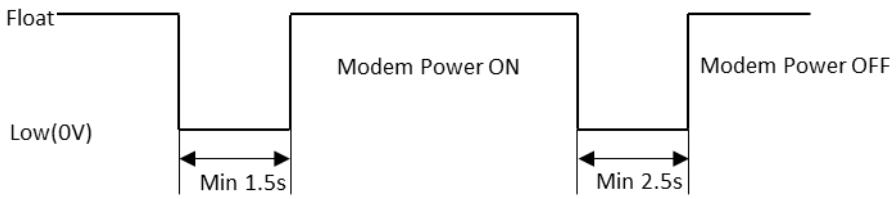


< Picture 6.3 Power Source example >

The module utilizes a single regulated power rail of DC typical 4.0V. The 4.0V power rail source must support to 550mA or more current. The module power must be supported to an independent power source. Noise, leakage current of output voltage and protection circuit should be considered when designing the power source.

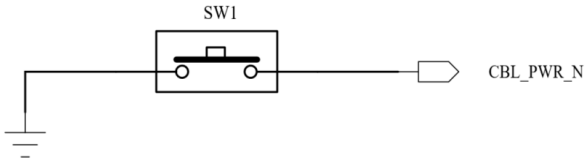
6.2 Power On Key

Picture 6.4.1 is power on sequence. CBL_PWR_N(pin 36) signal is an Active Low input that is used to turn on/off the module. When the input signal is Low for more than 0.5 sec while the module is turned off, the Module will be turned on. Conversely, When the input signal is Low for more than 1.5 sec while the module is turned on, the Module will be turned off.



<Picture6.2.1 >

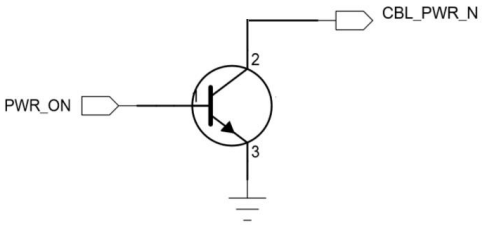
Tact type switch can be used to the module Power on/off design Power Key. Connect the switch to the CBL_PWR_N pin as shown in Picture 6.4.2.



<Picture6.2.2 >

When CBL_PWR_N pin is high input signal for 0.5 sec or 1.5 sec, it must be designed using a N-ch TR or FET to turn on/off the power. Refer to the picture 6.4.3.

CBL_PWR_N pin has internally 0.8V~ 1.0V pull-up.



<Picture6.2.3 >

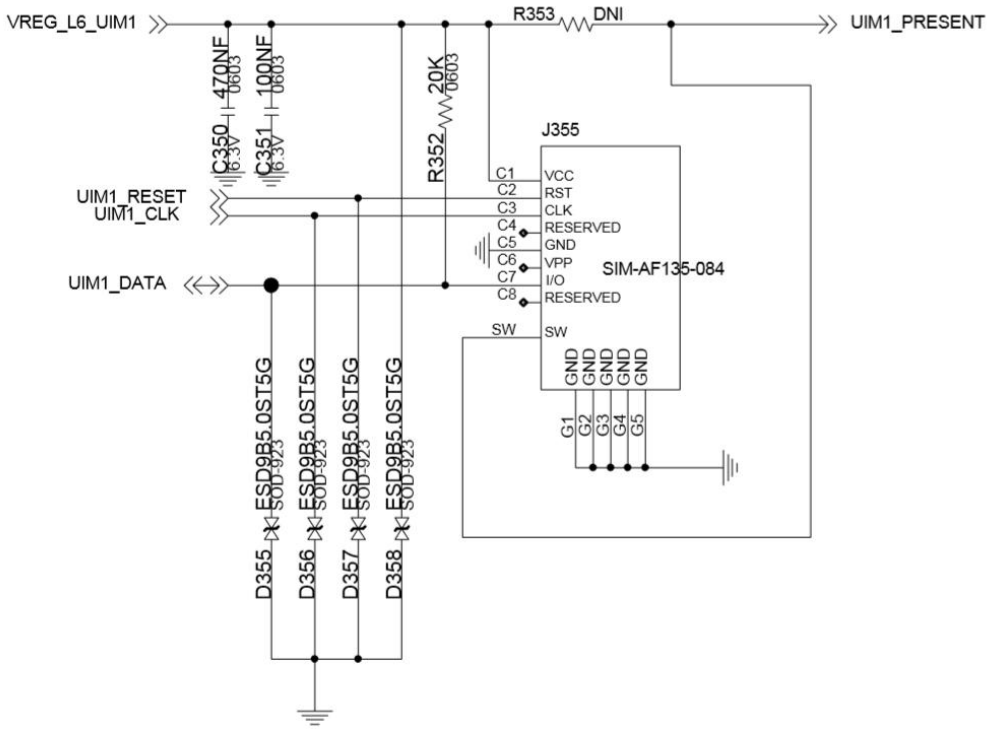
To design a power on without using power key or GPIO control, connect a pull-down resistor to CBL_PWR_N pin. In this case, the module does not operate in PSM mode.

6.3 UART Level Shifter

UART voltage level of the Module is 1.8V and 2.85V. It is recommended that UART Level shifter has control pin(enable/disable).

6.4 USIM Socket

UIM1_PRESENT pin(pin 52) is used to detect the insertion and removal for a SIM device in the SIM socket. When the SIM is inserted, the UIM1_PRESENT pin will transition from a logic 1 to a logic 0 state. It is recommended to ESD protection IC as TVS diode.



<Picture6.4 >

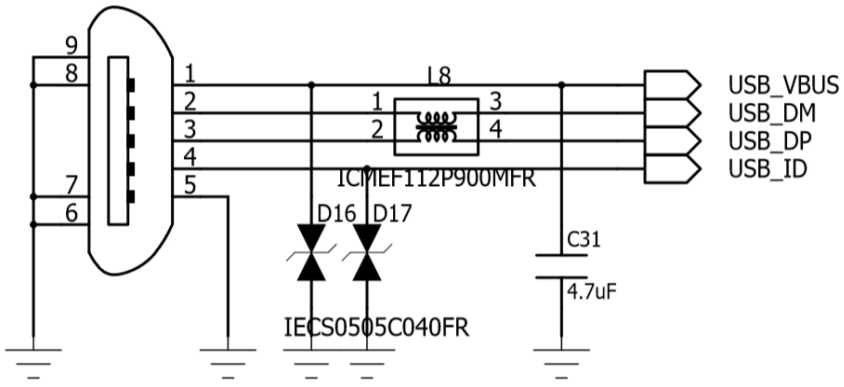
6.5 USB connection

USB_VBUS pin, USB_DP pin and USB_DM pin must be connected for a debugging purpose even if not used by the end application and USB interface.

It is recommended that the input signal of USB_VBUS is capable of on/off control in order to minimize the current consumption of the module. When USB VUSB input signal is supplied, sleep mode cannot be entered. When not in sleep mode, the current consumption is from 20mA to 30mA.

It is recommended to connect common mode ESD to USB interface lines.

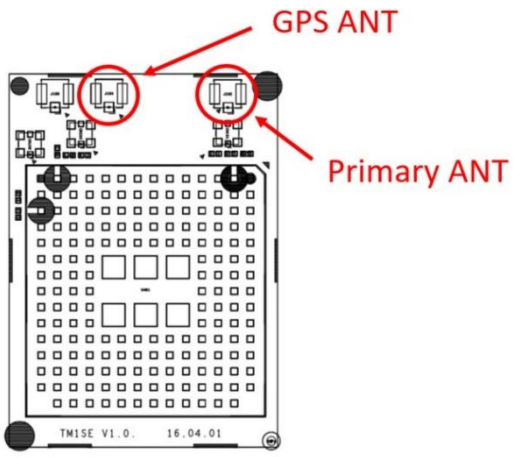
The impedance of USB differential trace is 90 Ω.



<Picture6.5 >

6.6 Antenna Block

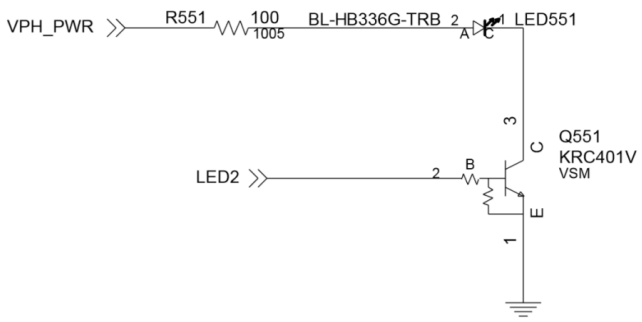
The Module has Main LTE Antenna connector and GPS Antenna connector.



<Picture6.6 >

6.7 Status LED

Two GPIOs(pin 42, pin 32) are for LED control. LED control circuit must be designed using TR or FET for sink current.



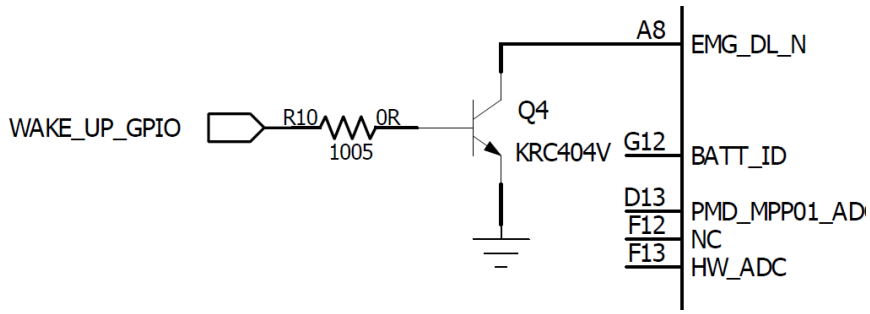
<Picture6.7 >

6.8 Wakeup interrupt GPIO

When the input signal is Low while the module is in sleep mode, the Module will be wake-up.

EMG_DL_N pin(pin 70) has internally 1.8V pull-up.

When ENG_DL_N pin is high input signal(over 1.8V), it must be designed using a N-ch TR or FET to turn on/off the power.



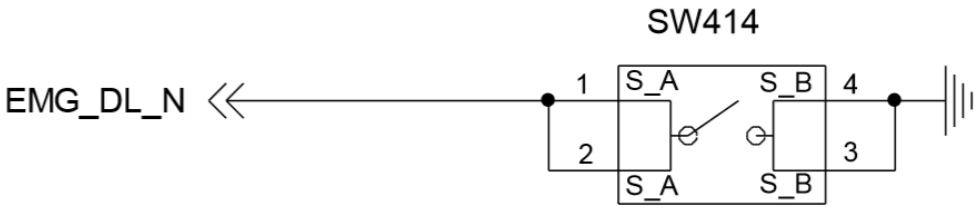
<Picture6.8>

6.9 Emergency download

EMG_DL_N pin(pin 70)=0 forces the module to Emergency download mode.

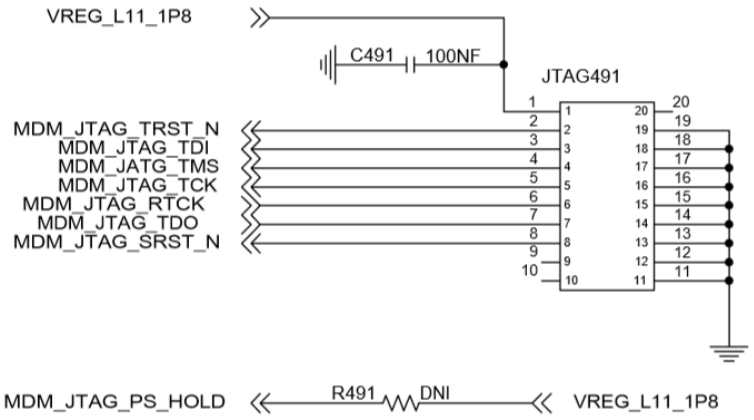
After boot, EMG_DL_N pin(pin A8) can be used for wakeup GPIO.

EMG_DL_N pin must be connected to TP or switch.



<Picture6.9>

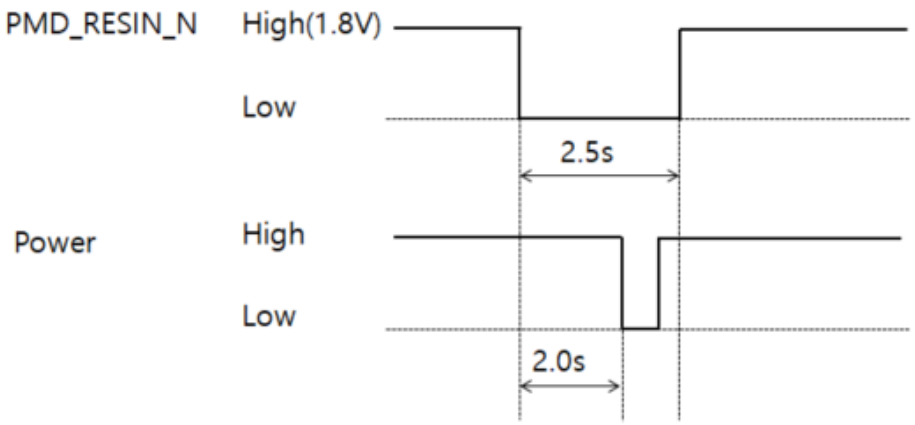
6.10 JTAG



<Picture6.10>

6.1 RESET

Asynchronous PMD_RESIN_N pin(pin 38), active low. Whenever this pin is active, the modem will immediately be placed in a Power On reset condition. PMD_RESIN_N pin has internally 1.8V pull-up.



<Picture6.11>